

Present Status of FE-D Submission

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Designs which are being prepared: proposed reticle

Status of Pixel Array Chip (FE-D): who is doing what, where

Next Steps and Tentative Schedule

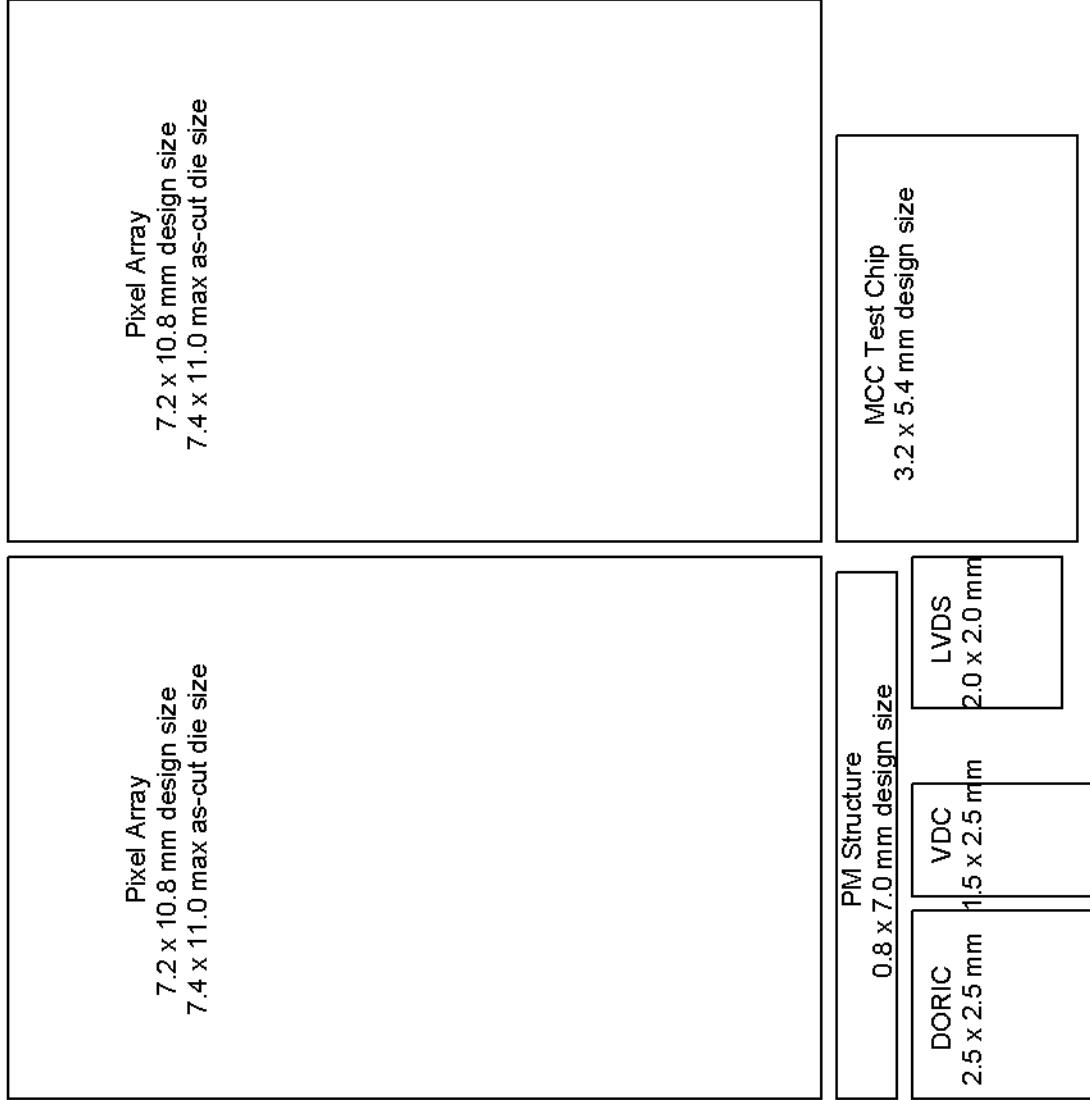
What Should be Included in FE-D Submission

Reticle is proposed to include a total of seven die:

- Two pixel array chips (FE-D).
- One Test Structure including basic W and L arrays for extracting SPICE models, and several devices that are identical to devices used in the FE-D pixel array and that might pose modeling problems. Responsibility: F. Pengg
- One LVDS buffer chip to replace the commercial LVDS translators presently need to interface a single pixel array to the PCC (a replacement for the rad-soft commercial components on the single-chip support card). Responsibility: L. Blanquart
- One prototype MCC chip in DMILL, to include one FIFO, the complete command decoder, and several other circuit blocks. Will also allow rad-hard module testing in transparent mode. Responsibility: Genova
- Three prototype opto-electronics chips, arranged on two die. One die will contain two CMOS versions of the DORIC opto-receiver chip (different biasing techniques), and the second die will contain a CMOS VDC. Responsibility: Siegen and OSU
- We will include all of these designs if they are ready when FE-D is ready....

Proposed Reticle Layout:

DMLL Reticle Layout (drawn to scale, 200 μ gap between designs)



Reticle approximately 14.6 x 14.5 mm. Expect this to give roughly 50 reticles per 6" wafer

Status of FE-D Pixel Array Chip

The analog parts:

- CPPM has delivered the front-end layout (preamp and discriminator), plus the LVDS I/O design, the bias cells, the current references, and the VCCD/VTH supply circuits. In some cases, the layout has been done by Bonn based on CPPM schematics. These blocks are all ready.

- The present layout uses the all-CMOS front-end design, similar to that of FE-C, but depending on new MAREBO test results, we may try once again to squeeze in the BiCMOS version of the front-end design. The BiCMOS version is about 13 μ longer, should have better timing and threshold dispersion performance, but relies on good beta for NPN after irradiation.

The digital parts:

- Bonn and LBL have worked closely on the digital readout. This includes the in-pixel circuitry, bottom-of-column circuitry for arbitration and buffering (sense amps for low-swing data transmission), the end-of-column, and the trigger FIFO, sequencer, subtractor, and serializer in the bottom of the chip.
- We suffered a major setback with the departure of the lead LBL designer on this (Atul Joshi) at the end of Feb. Bonn has helped to pick up the slack, but this has delayed other work they needed to do.

- In addition, several features of DMILL have caused us to invest significantly more time than was expected in completing this work.
- The first is the difficulty of integrating the required functions into the allowed space using only two metals and large NMOS of DMILL. There have been many iterations on the layout, including a major “squeeze” by Mario on the in-pixel and end-of-column circuitry (some weeks of work) which resulted in substantially smaller layout blocks. This gained enough space in the pixel to add digital injection capability, and transistor and bus size optimization. It may also still allow adding in the BiCMOS front-end (not quite enough space at present). It also gained enough space to include 24 EOC buffers instead of the 20 buffers originally planned.
- The second is the difficulty of engineering our designs to work with the DMILL “corner” models, particular the worst case “irradiated slow-slow”, which should represent the slowest performance of all devices to be expected after 25 MRad. This is more than a factor 2 slower than the “typical” performance which is in turn a factor two slower than the “fast” performance. Designing to meet our goal of operation with “iss” at 3.0V seems to be impossible, but operation at a slightly higher voltage should be OK (3.5V?). Many circuits underwent major revisions in design to meet these needs (often resizing resulted in a very non-optimal design). Also, some aspects of the design have been modified to reduce sensitivity to single-event upset (example is FIFO pointer management no longer done by shift register, but by actual counters).

- The present status is that all blocks have been completed except the sequencer. The complete column-pair (pixels, BOC logic and EOC logic) is being exercised now in Bonn with both Eldo and Verilog simulations, including corner simulations. The LBL engineer on this part (Roberto Marchesini) has spent the last several weeks in Bonn working on reaching this point.
- In response to these more global simulations, modest buffer size changes, etc. have been implemented, the speed of the EOC sparse-scan circuit has been improved, and a long-standing problem with simultaneous read-write access to EOC buffers has been fixed. This work will continue for several weeks until we are sure that the digital readout really does what it should.

Other parts:

- The DACs are a new design from Peter using a 2D array of current mirrors to provide a precise and rad-tolerant design.
- There is also a new “charge injection” scheme based on a steered current source that is being explored by Peter.
- The pixel control block, various registers, and the command decoder are also all Bonn contributions, and are completed. New features include parity checking on the single long Global Register which now contains all DACs and control bits, and column masking for the Pixel Register, the HitBus, and the Digital Readout under the control of a single bit per column-pair, plus true self-triggering.

Summary:

- The layout of almost all individual blocks is done (one remaining). Almost all blocks have been placed into the complete floorplan. The hard work being done recently in Bonn has included integrating the BOC region. This region includes the FE biasing for the analog block, the column-mask logic for the control block, and the arbitration and sense amps for the readout block. It is very challenging to integrate this with power bussing, etc. with 2 metal layers...
- We expect the layout work to be all completed by about the middle of June. We will have a two day “review” of the state of the submission in Bonn on June 9-10. This will be used to define the list of remaining tasks before submission. Before we have this discussion, it is difficult to predict the exact submission date, but it should be not later than early July.
- It is essential for this work that we thoroughly exercise the digital readout circuitry. Our strategy so far has been to use Verilog for initial bug finding and very large scale simulations. However, it requires a great deal of hand annotation, and it still does not include parasitics and drive strength issues in a reliable way. ELDO (SPICE) is being used for detailed timing and waveform simulations. However these simulations are slow, often special “chopped” layouts need to be created to increase speed for large simulations, and the outputs must be interpreted by hand.

- We are trying to add a new tool for this work, Timemill from Synopsys, and if this works well enough and soon enough, it may span the gap between the two approaches above.
- We will see in this meeting the status of the other designs for the FE-D submission, but they are probably not on the critical path.
- We will almost certainly provide the additional funding to TEMIC to accelerate the fabrication of this run (25 KCHF shortens the nominal turn time from 12 weeks to 8 weeks, but we have to see what this means when we overlap the summer maintenance shutdown of the TEMIC fab....).